

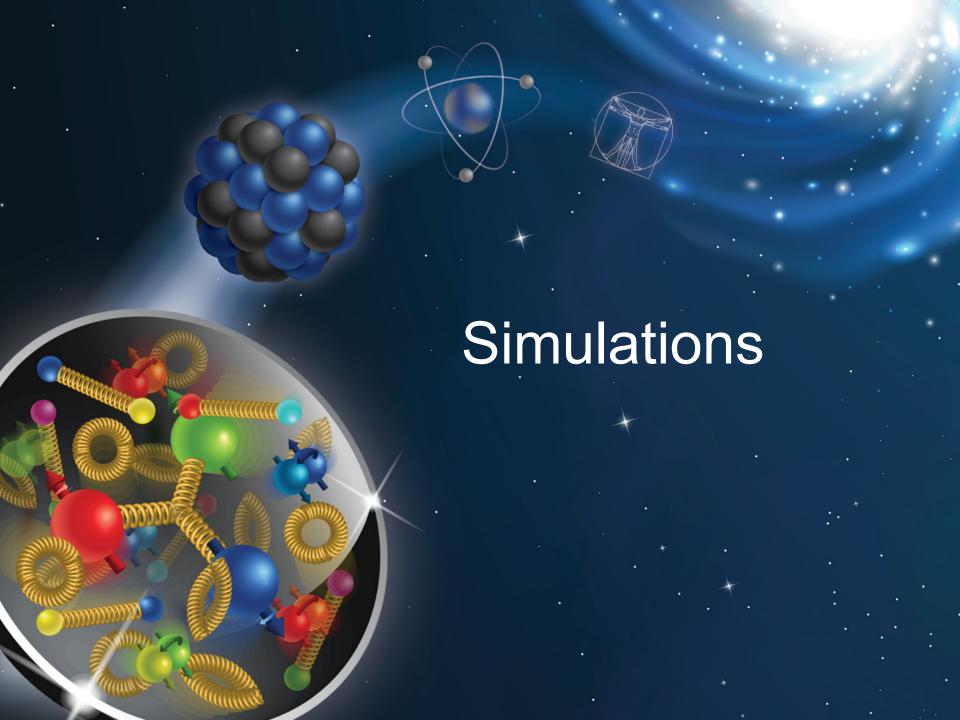
### 1st year R&D Proposal Goals and Approach

#### Goals:

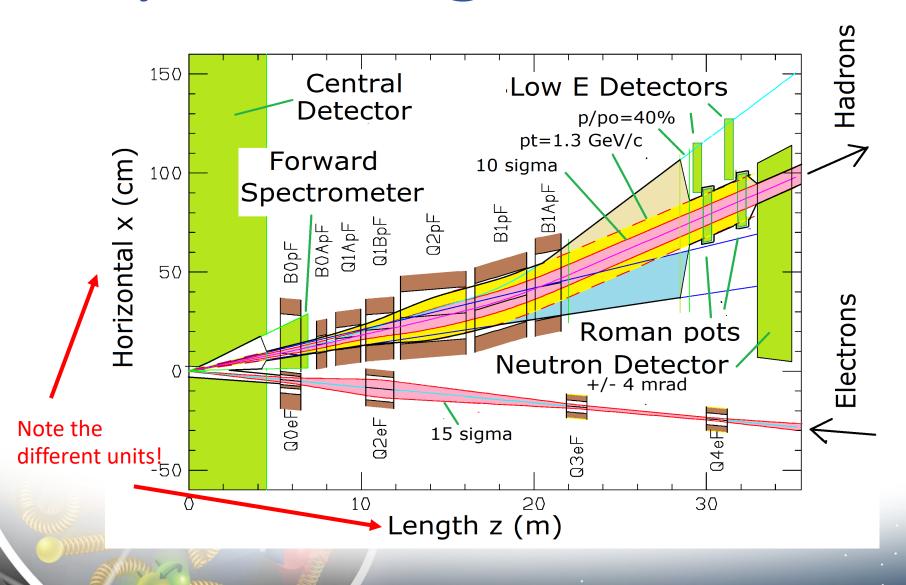
- Set performance requirements for Roman Pots at EIC
  - Focus on spatial granularity and timing resolution
- Study application of novel silicon sensor, AC-coupled LGAD, in Roman Pots at EIC
- o Compare with alternative detector option: 3D detector

#### Approach:

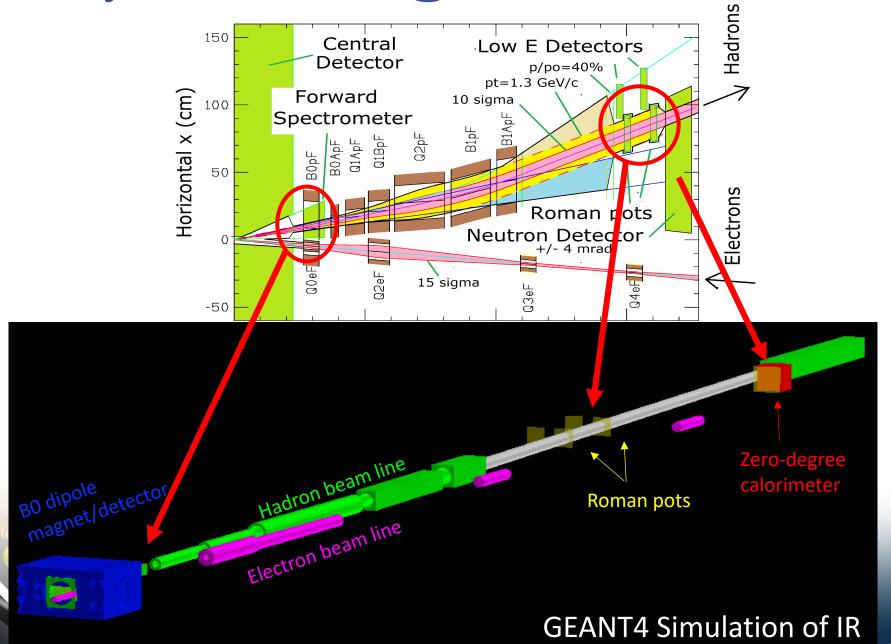
- o 1st year: physics performance simulation and sensor prototype development
  - Leverage BNL expertise on physics at RHIC
  - Leverage BNL expertise on silicon R&D, LGADs, and AC-LGADs
  - Leverage collaboration with Stony Brook/Manchester on 3D detectors
- o 2<sup>nd</sup> year: prototype testing at RHIC
  - Leverage RHIC resources for test-beam installation
  - Leverage expertise in Physics Dept. on pixel detector readout electronics



# IR Layout for EIC @ BNL detector

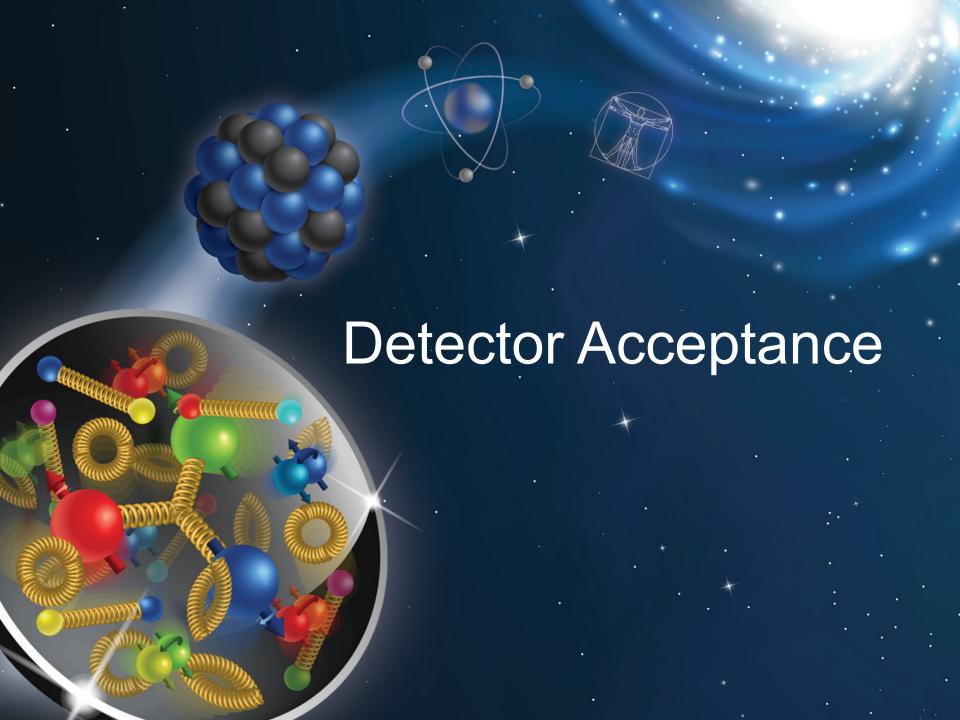


# IR Layout for EIC @ BNL detector

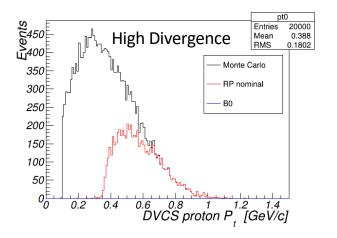


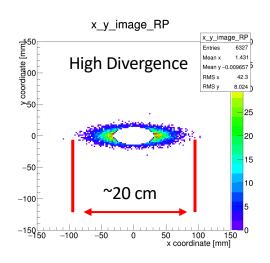
### **Full Simulations**

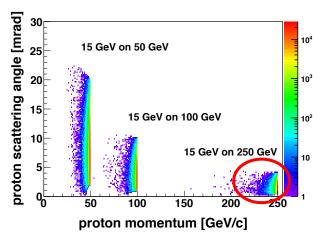
- e+p exclusive events generated using MILOU a generator of DVCS events.
- All machine elements, magnetic fields, detectors, etc. implemented in simulation using GEANT4.
- Various beam energies considered (5(e)x41(p) GeV, 10x100 GeV, 18x275GeV)
- Effects from beam angular divergence and vertex smearing from crab cavity rotation included.



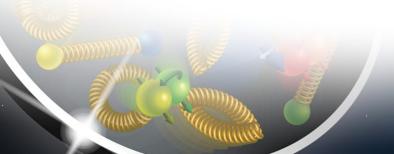
# 275 GeV DVCS Proton Acceptance



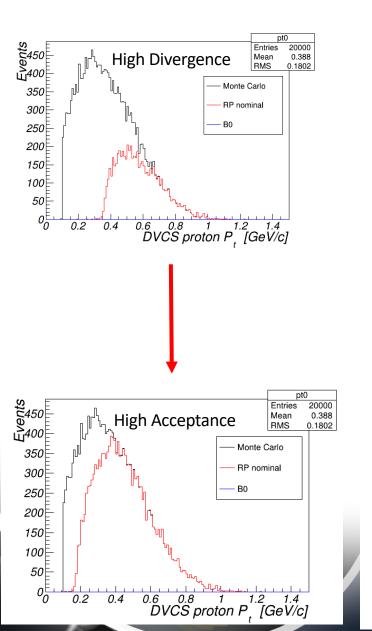


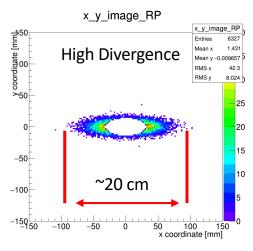


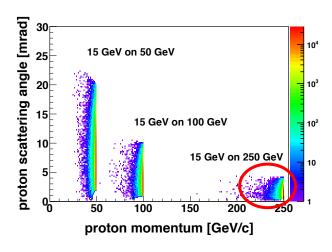
The high divergence configuration severely reduces the low  $p_t$  acceptance.

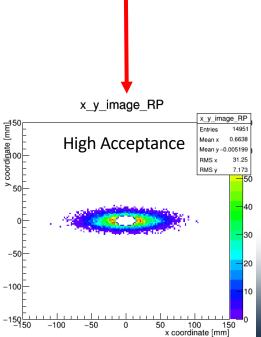


# 275 GeV DVCS Proton Acceptance





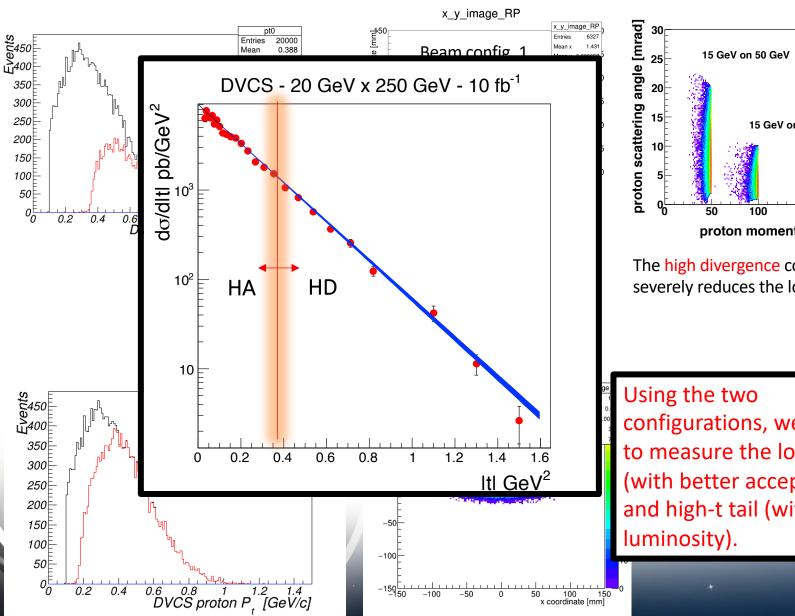


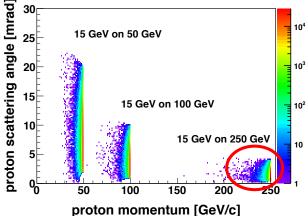


High Divergence: smaller  $β^*$  at IP, but bigger β(z = 30m) -> higher lumi., larger beam at RP

<u>High Acceptance:</u> larger  $\beta^*$  at IP, smaller  $\beta(z=30m)$  -> lower lumi., smaller beam at RP

# 275 GeV DVCS Proton Acceptance





The high divergence configuration severely reduces the low  $p_t$  acceptance.

configurations, we are able to measure the low-t region (with better acceptance) and high-t tail (with higher



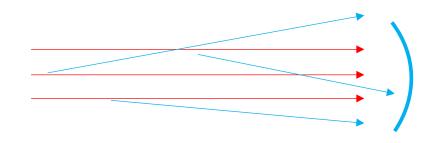
# Digression: particle beams

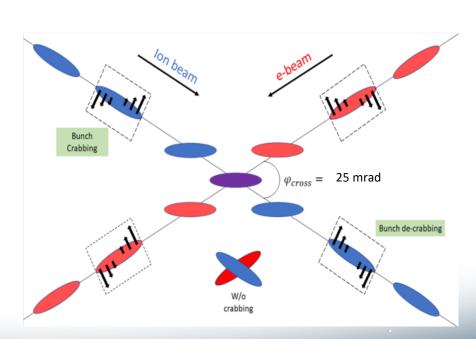
#### Angular divergence

- Angular "spread" of the beam away from the central trajectory.
- Gives some small initial transverse momentum to the beam particles.

#### Crab cavity rotation

- Can perform rotations of the beam bunches in 2D.
- Used to account for the luminosity drop due to the crossing angle – allows for head-on collisions to still take place.





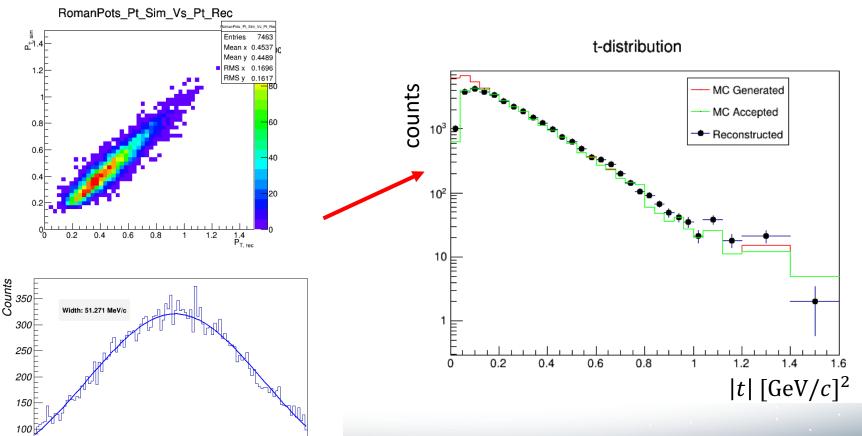
These effects introduce smearing in our momentum reconstruction.

### Momentum Resolution – 275 GeV

• Beam angular divergence (HD) ->  $\Delta p_t \sim$  40 MeV/c

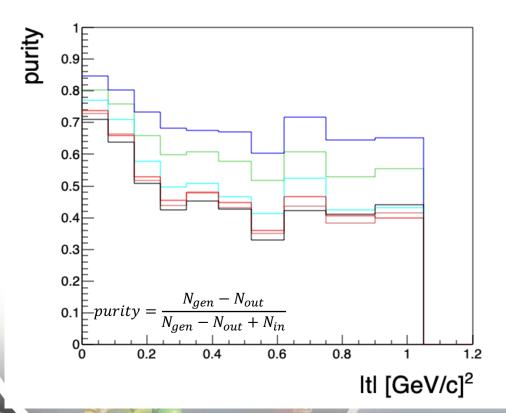
-0.06 -0.04

- Finite pixel size on sensor ->  $\Delta p_t \sim$  3 MeV/c to 25 MeV/c [55um x 55um to 1.3mm x 1.3mm].
- Vertex smearing from crab rotation->  $\Delta p_t \sim$  20 MeV/c removable with precise (~35ps) timing.



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#### Total smearing in p<sub>T</sub>:

- 30 MeV/c (HA + timing + 500um pxl)
- 38 MeV/c (HA + timing + 1.3mm pxl)
- 42 MeV/c (HD + timing + 500um pxl)
- 45 MeV/c (HD + no timing + 500um pxl)
- 51 MeV/c (HD + timing + 1.3mm pxl)
- 55 MeV/c (HD + no timing + 1.3mm pxl)

# Momentum Resolution – Timing

For exclusive reactions measured with the Roman Pots we need good timing to resolve the position of the interaction within the proton bunch. But what should the timing be?



Looking along the beam with no crabbing.

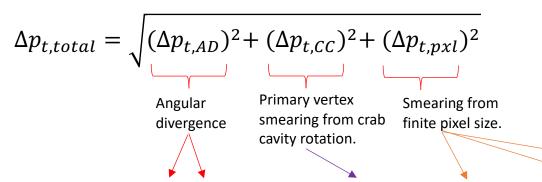


What the RP sees.

- Because of the rotation, the Roman Pots see the bunch crossing smeared in x.
- Vertex smearing = 12.5mrad (half the crossing angle) \* 10cm = 1.25 mm
- If the effective vertex smearing was **for a 1cm bunch**, we would have **.125mm** vertex smearing.
- The simulations were done with these two extrema and the results compared.
- From these comparisons, reducing the effective vertex smearing to that of the 1cm bunch length reduces the momentum smearing to negligible from this contribution.
   This can be achieved with timing of ~ 35ps (1cm/speed of light).

### Momentum Resolution - Comparison

 The various contributions add in quadrature (this was checked empirically, measuring each effect independently).



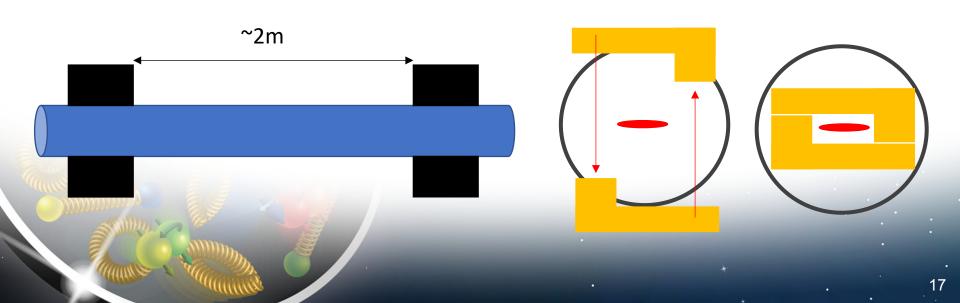
| $\Delta p_{t,total}$ [MeV/c] - 275 GeV |
|----------------------------------------|
| $\Delta p_{t,total}$ [MeV/c] - 100 GeV |
| $\Delta p_{t,total}$ [MeV/c] - 41 GeV  |

| Ang Div. (HD) | Ang Div. (HA) | Vtx Smear | 250um pxl | 500um pxl | 1.3mm pxl |
|---------------|---------------|-----------|-----------|-----------|-----------|
| 40            | 28            | 20        | 6         | 11        | 26        |
| 22            | 11            | 9         | 9         | 11        | 16        |
| 14            | -             | 10        | 9         | 10        | 12        |

- Beam angular divergence
  - Beam property, can't correct for it sets the lower bound of smearing.
  - Subject to change (i.e. get better) beam parameters not yet set in stone
- Vertex smearing from crab rotation
  - Correctable with good timing (~35ps)
- Finite pixel size on sensor
  - 500um seems like the best compromise between potential cost and smearing

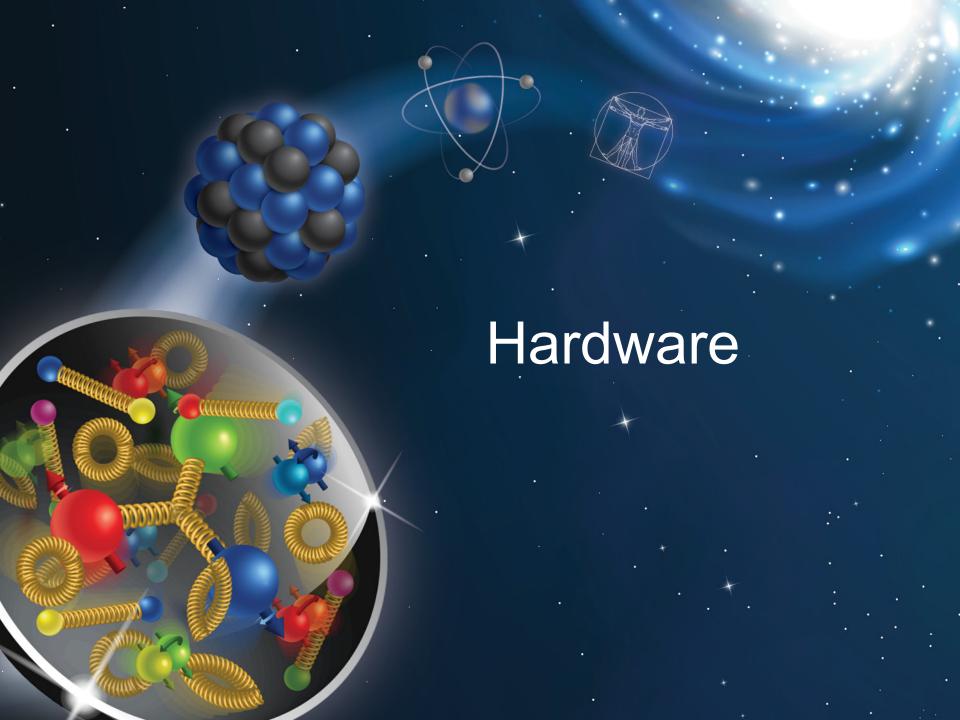
# Possible Layout

- Two stations, separated by ~ 2 meters.
- 2-3 layers of sensors per station for redundancy – square pixels.
- L-shaped sensor pattern could allow the  $2\pi$  coverage needed.



# Summary of Simulation Findings

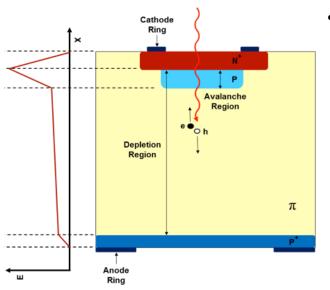
- The EIC Roman Pots will require an active sensor area of ~25cm x 10cm.
- The beam angular divergence sets the lower bound for achievable smearing other controllable effects should be kept well-below contribution from divergence.
- We find that a 500um x 500um sensor pixel is the best trade-off between introduced smearing and cost.
- Having precise timing ~35ps allows for precise determination of z-position of collision relative to the center of the bunch.



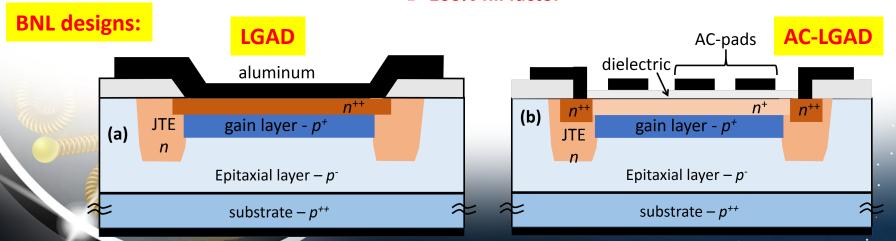
### Progress on detector development for RPs

- Studies of AC-LGAD performance compared to LGADs
  - Signal collection, signal induced on adjacent pixels, timing performance
- New AC-LGAD production for RP application at EIC
  - Slim edges, various designs with varied geometrical and fabrication details
- Towards an RP detector
  - Discussion on readout options

#### Time and Space with AC-LGADs



- A highly doped, thin layer of *p*-implant near the *p-n* junction in silicon creates a high electric field that accelerates electrons enough to start multiplication (*gain*).
  - Low Gain Avalanche Detectors (LGADs):
    - Gain 5-100
    - 50 μm thickness
    - Large S/N ratio
    - Fast-timing: ~30-50 ps per hit
    - Rad-hard up to 3x10<sup>15</sup> 1 MeV neutron/cm<sup>2</sup>
    - To be used in forward timing det. at ATLAS and CMS at HL-LHC
- Novel development: AC-coupling allows fine segmentation
  - Time & Space measurements
  - → 100% fill factor



#### AC-LGADs Fabrication at BNL

- BNL is fabricating and testing LGADs and AC-LGADs for several applications
- G. Giacomini, A. Tricoli et al., "Development of a technology for the fabrication of Low-Gain Avalanche Detectors at BNL", NIMA 62119 (2019)
- G. Giacomini, A. Tricoli et al., "Fabrication and performance of AC-coupled LGADs", arXiv:1906.11542 (2019), sub. to JINST

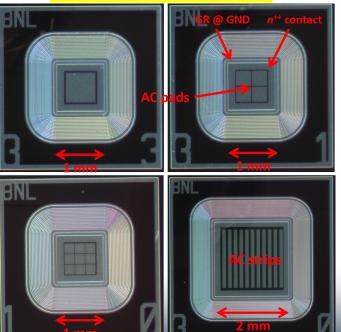
#### BNL's LGAD show performance similar to HPK

leakage current 1nA/cm²

High gain, up to ~80

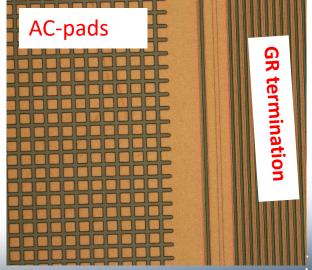
**BNL's LGAD Wafer** 





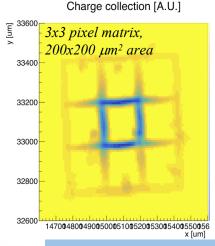
**Single-pad** (1x1 mm2) and **multi-strip/pixel** structures of several dimensions.

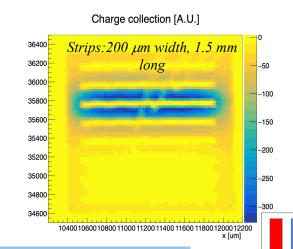
Smallest pitch: **55 um x 55 um** compatible with commercial readout chips

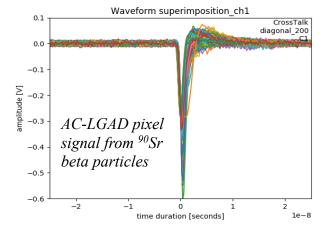


### Studies of AC-LGAD performance

- Characterization of AC-LGADs of different pitches and for several applications, including RPs for EIC
  - o Response to different particle beams: Beta, X/gamma rays, red/IR lasers, neutrons
  - Electrical and charge collection properties
  - Signal induced on adjacent pixels/strips vs implant dose
  - Time resolution: ~20 ps jitter







Charge collection through IR Laser scan (TCT)

Improved and optimized performance expected in next batches

#### Charge sharing can help improve spatial resolution

|  | Amplitude <sub>2</sub> / Amplitude <sub>1</sub> | 100% |
|--|-------------------------------------------------|------|
|  | Amplitude <sub>3</sub> / Amplitude <sub>1</sub> | 13%  |
|  | Amplitude <sub>4</sub> / Amplitude <sub>1</sub> | 6%   |
|  | Amplitude <sub>6</sub> / Amplitude <sub>1</sub> | 4%   |

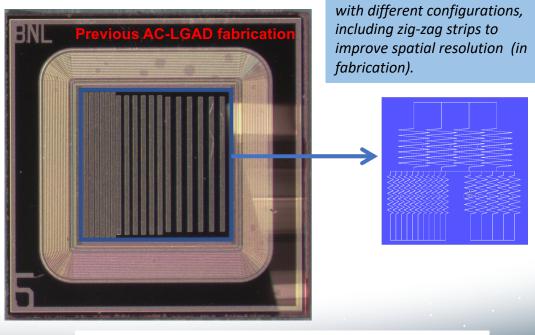
### AC-LGAD design and production for RPs

- New designs in upcoming wafer productions to address RP-specific requirements
  - Slim edge design: inactive edge area to be reduced to 50-100 μm
  - Optimized configurations to study induced signal on adjacent pixels/strips

Test Structure for HV capability tests, one guard ring only for Slim Edge studies



- Prelim. Results: slim edge of 100 μm is within reach
  - 35-40 µm pad to Guard Ring
  - 50 μm Guard ring to etched trench

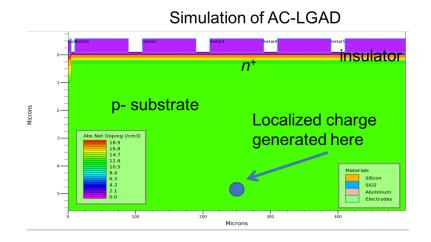


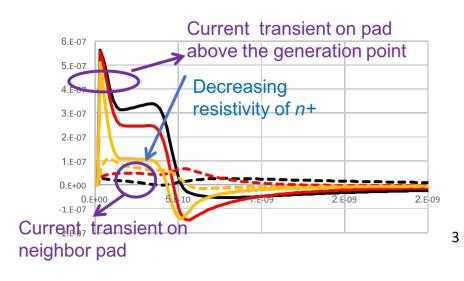
Performance of such structures will be compared with standard designs

Several chips in a few wafers

#### Improvement on spatial resolution

- Cluster centroid can be measured by induced signal on adjacent pixels/strips
- Critical parameters are geometry and fabrication details (doping, oxide thickness) that impact macroscopic quantities e.g. RC
- Ongoing studies on TCAD simulation to explore large parameter space



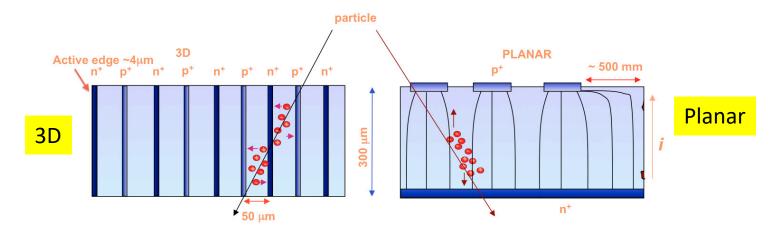


Signal fed to the read-out electronics strongly depends on R(C):

- Higher crosstalk if RC is SMALL
- Higher signal on hit pad if RC is HIGH

The RC value is being studied and tuned during fabrication to have an acceptable compromise

#### Comparison with 3D sensors



#### Charge collection in LGADs and 3D:

- o a 3D collects 80 e-/h pairs x 200μm → ~ 16k e-/h pairs
- o an LGAD collects 80 e-/h pairs x 50 $\mu$ m x Gain  $\rightarrow$  80k e-/h pairs (at a Gain  $\sim$  20, higher has been achieved)
- $\circ$  since drift length is 50  $\mu m$  for both, current signal is higher for LGAD
- Capacitance/Area is much higher in 3D
- We performed tests with a charge sensitive preamplifier first.
- Charge from 3D lower than expected but results where probably affected by large capacitance of the 3D.
- Set-up to be upgraded.

### Towards an RP detector

- Possible test-runs in Spring to study sensor performance with proton beams
  - Tests of charge collection and charge sharing with old and new AC-LGAD designs
- A critical aspect of the detector design is the readout electronics
  - ASIC for ATLAS and CMS fast-timing detectors ALTIROC and ETROC chips
    - 225 and 256 channels, and 130 nm and 65 nm technology, respectively
    - TDCs for TOA and TOT, and RAMs for data buffering
    - ~25 ps jitter for 10 fC charge, power consumption 200-300 mW/ cm²
  - Discussion has started with ALTIROC and ETROC ASIC designers
    - Current ASIC feature sizes are limited by TDCs and RAM sizes
    - Possible to adapt current designs for ~500x500 μm² feature size at similar performance, with limited effort by expert designer (block rearrangements, removal/optimization of components, e.g. large RAM).
    - Slim edges of 50-100  $\mu m$  on three sides (out of four) of the ASICs can be achieved
    - TOT feature in ASICs may be used to measure charge collected and shared between pixels to improve spatial resolution beyond pixel pitch size.

### Questions towards TDR

- How much time do you envision to complete your ongoing project
  - FY20 to complete physics/performance studies and sensor R&D
  - FY21 for prototype sensor device and dedicated tests
  - FY21-23 for readout design
- What achievements are required for TDR readiness 2023
  - Need to develop detailed detector layout and readout strategy
  - Need to include ASIC designers to develop readout strategy

### Conclusions and Outlook

#### Area of progress in the first 6 months of project:

#### Setting detector requirements

- > Strawman layout: 2 stations with 2-3 layers each, with active area per layer of 25 x 10 cm<sup>2</sup>
- > 500 x 500 μm² pixel area allows to meet physics performance goals
- > ~35 ps time resolution per hit is the target

#### Detector R&D

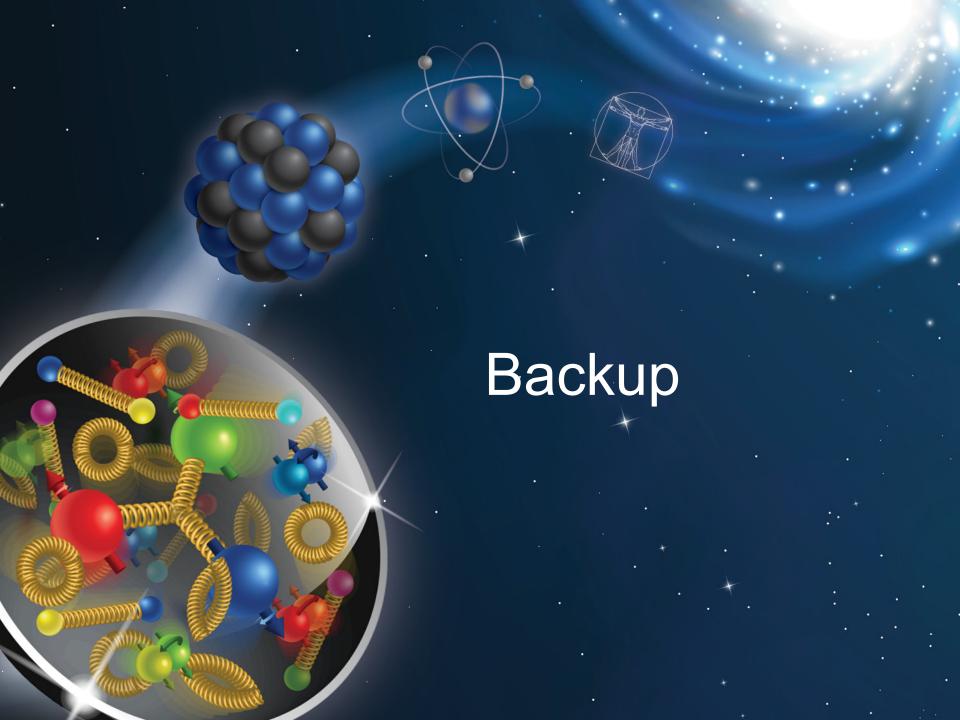
- Studies show that slim edges of 100 μm or less are possible
- Studies show that AC-LGADs with pixel area 500 x 500 μm² or less can be fabricated with performance compatible to standard LGADs
- Dedicated AC-LGAD designs with various geometrical layouts and different fabrication details (doping) are studied and implemented in ongoing productions
- Comparison with 3D sensors is ongoing

#### Exploration of algorithms to improve spatial resolution beyond pixel size

cluster centroid can be measured by induced signal on adjacent pixels

#### Plans for the remainder of FY20

- Conclude analysis of main detector requirements
- Complete AC-LGAD production with new sensors designed for RPs, and associated testing at BNL
- Possible test-beams for AC-LGADs
- AC-LGAD performance comparison with 3D detectors
- Continue discussion with ASIC designers

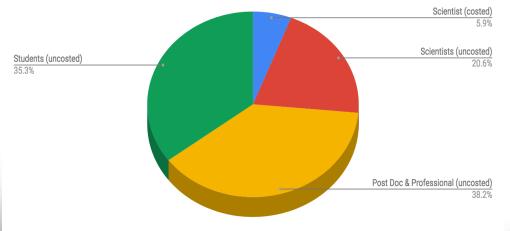


#### Tasks and Deliverables

- Define set of requirements for time resolution, geometrical layout (including non-active region) such that the acceptance of the forward scattered particles is not impacted
- Fabrication of three batches of AC-LGADs with different designs for optimization studies for Roman Pots
  - o Main focus will be on small-size LGAD edges
    - 1st batch: AC-LGADs with fewer guard rings to establish minimum edge size for safe operations
    - 2<sup>nd</sup> batch: small-edge AC-LGADs with different geometrical layouts, e.g. pixel no. and pitch
    - 3<sup>rd</sup> batch: optimized AC-LGAD design that best matches final requirements that are set by physics studies
- Comparison of performance of optimized AC-LGAD and 3D sensors
  - 3D detectors provided by SBU/Manchester
  - Compare timing and edge size in both detectors
- Assessment of pro's and con's of AC-LGADs and 3D technologies based on scientific requirements, integration into the accelerator, cost, schedule and operations for application in Roman Pots at an EIC

# Manpower and Budget

- Leveraging of equipment and resources available in Physics Dept. and Instrum. Div.
  - Clean room for Silicon fabrication
  - Equipped lab for fast-timing silicon sensor characterization
  - Interconnect lab for wire/bump bonding and metrology
  - Synergy with A. Tricoli Early Career Award and LDRD: support of labor for AC-LGAD and 3D detector testing
  - Synergy with E.C. Aschenauer 3-year program development "eRHIC: from Virtual to Real": support
    of labor for simulations



| Costed Item | Direct Cost [\$] |
|-------------|------------------|
| Labor       | 20,000           |
| M&S         | 10,000           |
| Travel      | 5,000            |
| Total       | 35,000           |

- Costed Labor: 0.10 FTE scientist for AC-LGAD design and fabrication in clean room
- **M&S:** consumables for 3 AC-LGAD batch productions (e.g. wafers and masks)
- Travel: student travel to BNL for 2 month for 3D detector testing

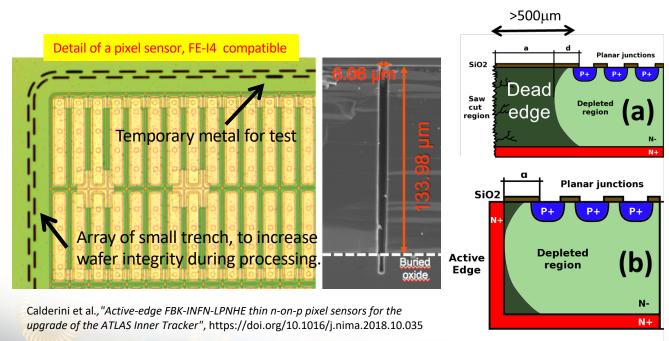
# ALTIROC

| TID tolerance                         | Inner region: 4.7 MGy                                                                                            |  |
|---------------------------------------|------------------------------------------------------------------------------------------------------------------|--|
|                                       | Outer region: 2.0 MGy                                                                                            |  |
| Pad size                              | $1.3 \times 1.3 \mathrm{mm}^2$                                                                                   |  |
| Voltage                               | 1.2 V                                                                                                            |  |
| Power dissipation per area (per ASIC) | $300 \mathrm{mW} \mathrm{cm}^{-2} (1.2 \mathrm{W})$                                                              |  |
| e-link driver bandwidth               | $320 \mathrm{Mbit}\mathrm{s}^{-1}$ , $640 \mathrm{Mbit}\mathrm{s}^{-1}$ , or $1.28 \mathrm{Gbit}\mathrm{s}^{-1}$ |  |
| Temperature range                     | −40 °C to 40 °C                                                                                                  |  |
| SEU probability                       | < 5%/hour                                                                                                        |  |

| Maximum leakage current           | 5μA                              |  |
|-----------------------------------|----------------------------------|--|
| Single pad noise (ENC)            | $< 1500 e^{-} = 0.25 \text{ fC}$ |  |
| Cross-talk                        | < 5%                             |  |
| Cross will                        | , -                              |  |
| Minimum threshold                 | 1fC                              |  |
| Threshold dispersion after tuning | 10%                              |  |
| Maximum jitter                    | 25 ps at 10 fC                   |  |
| TDC contribution                  | < 10 ps                          |  |
| Time walk contribution            | < 10 ps                          |  |
| Dynamic range                     | 2.5 fC-100 fC                    |  |
| TDC conversion time               | < 25 ns                          |  |
| Trigger rate                      | 1 MHz L0 or 0.8 MHz L1           |  |
| Trigger latency                   | 10 μs L0 or 35 μs L1             |  |
| Clock phase adjustment            | 100 ps                           |  |

# Edge studies for Roman Pots: DRIE etching technique

- Non-sensitive area (edges) is critical for their applications in a Roman Pot
  - Current AC-LGADs have large non-active region → need optimization for application in Roman Pots
- Active edge provides a damage free interface that limits the extension of the dead silicon area, external to the sensitive
  area
  - o To be studied for AC-LGADs and compared to 3D detectors



**Deep reactive ion etching** technique provides low-damage trenches or columns in silicon.

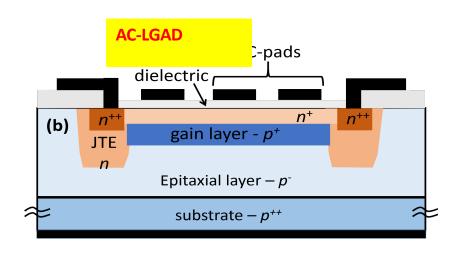
1:20 etch ratios are achievable. Any shape can be achieved.

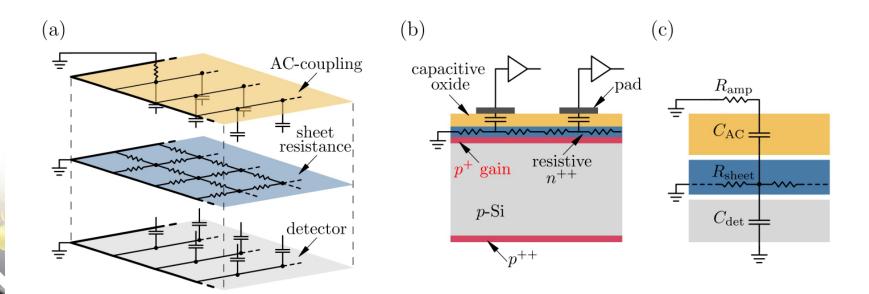
Surface needs passivation for damage removal, e.g. thermal oxidation.

To fabricate an active edge sensor, trenches must be etched all the way through the active thickness:

- For AC-LGADs, just 50 μm deep
- For 3D pixel sensors, ~ 200 μm

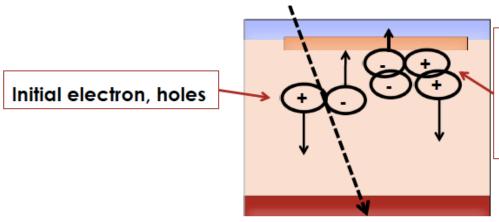
# AC-coupled LGAD





#### Charge Multiplication in LGADs

N. Cartiglia

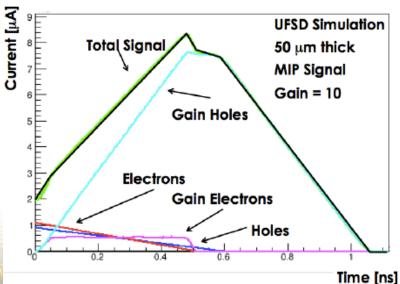


Gain electron:

absorbed immediately

Gain holes:

long drift home



Electrons multiply and produce additional electrons and holes.

- Gain electrons have almost no effect
- Gain holes dominate the signal
- → No holes multiplications

### Time Resolution in LGADs

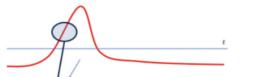
N. Cartiglia

$$\sigma_{\rm t} = (\frac{\rm N}{{\rm dV/dt}})^2 + ({\rm Landau~Shap})^2$$

Usual "Jitter" term
Here enters everything that
is "Noise" and the
steepness of the signal

**Time walk**: Amplitude variation, corrected in electronics

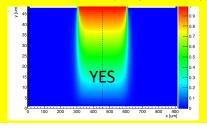
**Shape variations**: non homogeneous energy

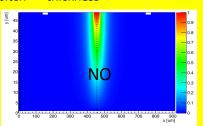




#### Signal Shape: i∝qvE<sub>w</sub>

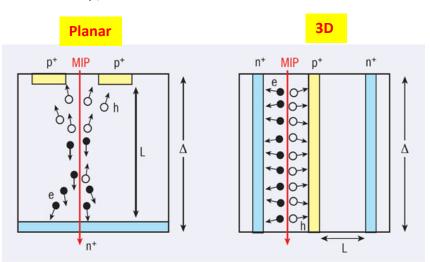
- Key to good timing is the uniformity of signals:
  - Drift velocity and field need to be as uniform as possible
  - Parallel plate geometry is optimal:
    - strip implant ~ strip pitch >> thickness





## Alternative: 3D detector

- 3D detectors are an alternative detector, already considered by current forward phys. experiments, e.g.
   CMS CT-PPS, AFP
  - Established technology for rad-hard tracking detectors, e.g. ATLAS inner pixel (IBL), and ITK for HL-LHC
  - $\circ$  Fast-timing performance (~30 ps for 50x50  $\mu$ m<sup>2</sup> pixels) and active edges
- Drawbacks:
  - Complex fabrication, expensive technology with only few major vendors so far (CNM- Spain, FBK -Italy)



#### Main 3D detector characteristics:

- o electric field is parallel to the wafer's surface
- o 100% fill factor
- o short inter-electrode distance
  - · reduced collection time
  - lower trapping probability after irradiation → rad-hard
  - small inactive edges by design

G. Kramberger et al., Timing performance of small cell 3D silicon detectors", NIMA 934 26-32
CT-PPS TDR: https://cds.cern.ch/record/1753795
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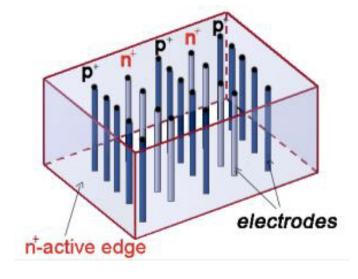
#### > Timing resolution depends strongly on the cell size and track inclination

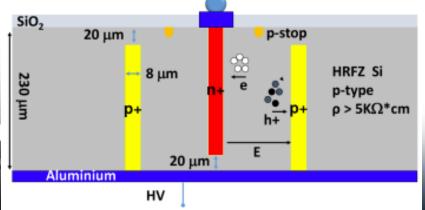
- Dominant contribution: different induced current pulse shapes due to hit position
- **High capacitance increases noise and time jitter** and should be carefully optimized in terms of number of electrodes and thickness for the required performance
  - 20 pF/mm<sup>2</sup> for 50x50μm2 cells, 300 μm thick detector,
  - o compared to 2-3 pF/mm<sup>2</sup> for 50 μm thick LGAD detector.
- Careful optimization of detection efficiency, noise occupancy and time resolution is required and may yield a different design than that for tracking detector only

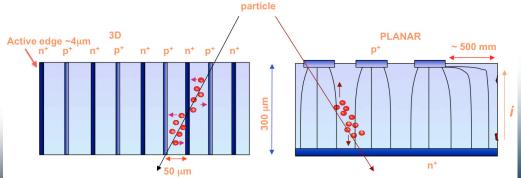
### ITk Pixel Technologies: 3D

#### 3D Silicon detectors: radiation-hard sensor technology

- Electrode distance decoupled from thickness
  - → smaller drift distance
  - → faster charge collection
  - → less trapping
  - → radiation hardness
- lower V<sub>depletion</sub> → less power dissipation, cooling
- Active or slim edges are natural feature of 3D technology



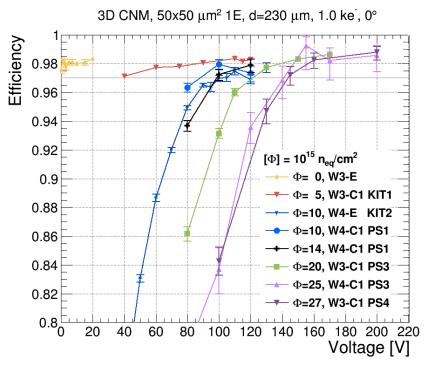




### ITk Pixel Technologies: 3D

#### Challenges

- Complex production process
  - → long production time
  - → lower yields
  - → higher costs
- Higher capacitance
  - → higher noise
- Non-uniform response from 3D columns and low-field regions
- → small efficiency loss at vertical incidence



J. Lange et al., 13thTrento Workshop 2018, publ. in prep.

- ➤ 3D prototypes successfully tested to unprecedented fluences: 3 x 10<sup>16</sup> neutron<sub>eq</sub>/cm<sup>2</sup> (beyond ITk fluences)
- Unprecedented radiation hardness of 3D pixel detectors demonstrated

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#### Generic solution adaptable to many experiments in a cost-effective manner Electronics for high-throughput detector readout & data acquisition

factorize front-end electronics from data handling...scalable, low maintenance, and easily upgradeable high-density data flow...up to 48 duplexed optical channels @ 10 Gb/s with 100 Gb/s over PCle gen3 easily adapted to external timing systems...LHC, RHIC, White Rabbit with <5 ps jitter network agnostic...works with most commodity network solutions (NIC) no special cooling required...approx. 50 W power consumption remote management...update firmware over network compact hardware...standard PCle card minimal infrastructure investment...works in most PCs! extensive support...ANL, BNL, FNAL, Irvine, CERN, NIKHEF, Weizmann



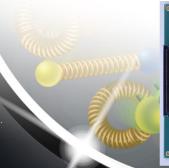






# Control & Readout Board (CaRIBOu)

- Modular readout system for HV-CMOS sensor R&D
  - open architecture with ZYNQ SoC to simplify firmware & software
  - easily adapted to various sensors under development
  - carefully defined interface to minimize design revisions
  - used in several test beams with FELIX readout at CERN
  - outgrowth of LDRD efforts
  - interest from NASA for this technology and for CLIC testbeams
- CaRIBOu with FELIX adapted for ATLAS HL-LHC ITk tests
  - important for final development of readout chains



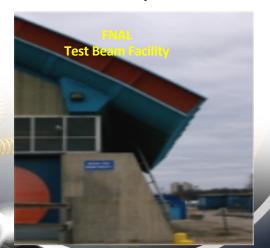






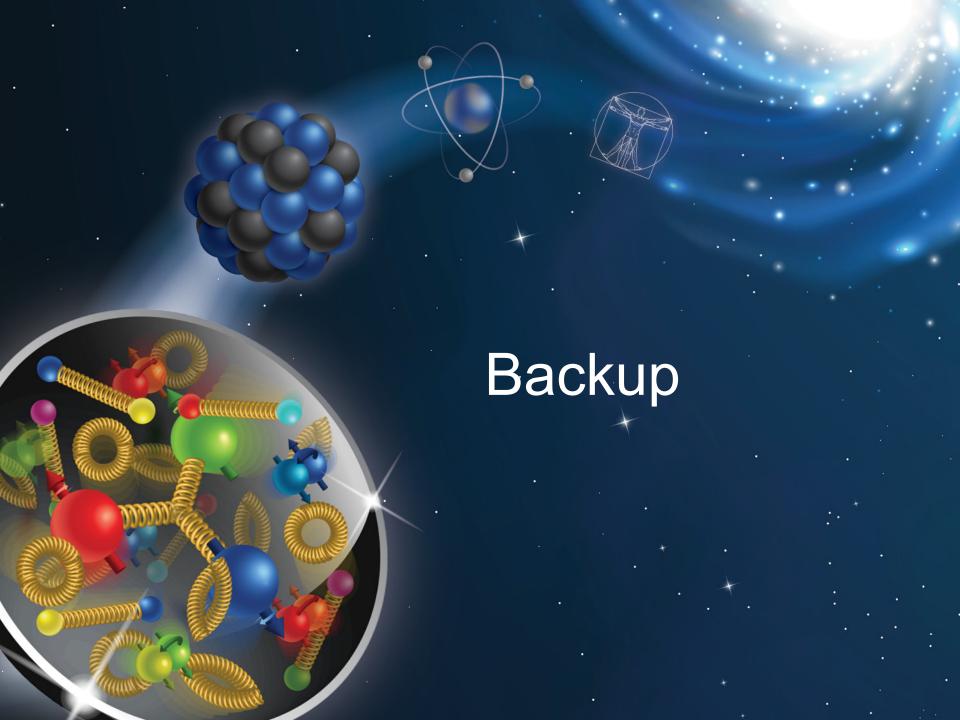
## FELIX and Caribou for Test Beams

- FELIX used with CaRIBOu for several test beams at FNAL & CERN
  - trigger rate reaches 60+ kHz much faster than previously available readout system (4 kHz)
  - outgrowth of LDRD effort
  - CERN: AMS180V4/5, H35Demo
  - FNAL: H35Demo, ATLASPix
- FELIX-based DAQ system in Fermilab Test Beam Facility (FTBF)
  - BNL provides **FELIX**-based hardware and firmware support
  - FNAL provides artDAQ-based software support
  - HV-CMOS sensors are the first targeted test-beam experiment



BNL's FELIX DAQ & CaRIBOu calibration boards used in this CERN test beam



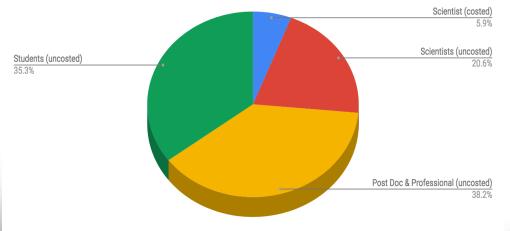


## Tasks and Deliverables

- Define set of requirements for time resolution, geometrical layout (including non-active region) such that the acceptance of the forward scattered particles is not impacted
- Fabrication of three batches of AC-LGADs with different designs for optimization studies for Roman Pots
  - Main focus will be on small-size LGAD edges
    - 1st batch: AC-LGADs with fewer guard rings to establish minimum edge size for safe operations
    - 2<sup>nd</sup> batch: small-edge AC-LGADs with different geometrical layouts, e.g. pixel no. and pitch
    - **3**<sup>rd</sup> **batch**: *optimized AC-LGAD design* that best matches final requirements that are set by physics studies
- Comparison of performance of optimized AC-LGAD and 3D sensors
  - 3D detectors provided by SBU/Manchester
  - Compare timing and edge size in both detectors
- Assessment of pro's and con's of AC-LGADs and 3D technologies based on scientific requirements, integration into the accelerator, cost, schedule and operations for application in Roman Pots at an EIC

# Manpower and Budget

- Leveraging of equipment and resources available in Physics Dept. and Instrum. Div.
  - Clean room for Silicon fabrication
  - Equipped lab for fast-timing silicon sensor characterization
  - Interconnect lab for wire/bump bonding and metrology
  - Synergy with A. Tricoli Early Career Award and LDRD: support of labor for AC-LGAD and 3D detector testing
  - Synergy with E.C. Aschenauer 3-year program development "eRHIC: from Virtual to Real": support
    of labor for simulations



| Costed Item | Direct Cost [\$] |
|-------------|------------------|
| Labor       | 20,000           |
| M&S         | 10,000           |
| Travel      | 5,000            |
| Total       | 35,000           |

- Costed Labor: 0.10 FTE scientist for AC-LGAD design and fabrication in clean room
- **M&S:** consumables for 3 AC-LGAD batch productions (e.g. wafers and masks)
- Travel: student travel to BNL for 2 month for 3D detector testing

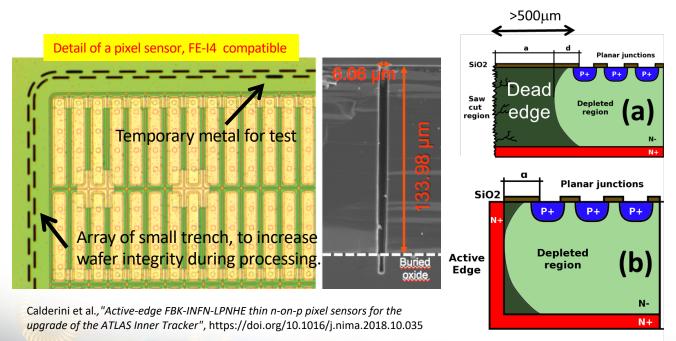
# ALTIROC

| TID tolerance                         | Inner region: 4.7 MGy                                                                                            |
|---------------------------------------|------------------------------------------------------------------------------------------------------------------|
|                                       | Outer region: 2.0 MGy                                                                                            |
| Pad size                              | $1.3 \times 1.3 \mathrm{mm}^2$                                                                                   |
| Voltage                               | 1.2 V                                                                                                            |
| Power dissipation per area (per ASIC) | $300 \mathrm{mW} \mathrm{cm}^{-2} (1.2 \mathrm{W})$                                                              |
| e-link driver bandwidth               | $320 \mathrm{Mbit}\mathrm{s}^{-1}$ , $640 \mathrm{Mbit}\mathrm{s}^{-1}$ , or $1.28 \mathrm{Gbit}\mathrm{s}^{-1}$ |
| Temperature range                     | −40 °C to 40 °C                                                                                                  |
| SEU probability                       | < 5%/hour                                                                                                        |

| Maximum leakage current           | 5µA                              |
|-----------------------------------|----------------------------------|
| Single pad noise (ENC)            | $< 1500 e^{-} = 0.25 \text{ fC}$ |
| Cross-talk                        | < 5%                             |
| Minimum threshold                 | 1fC                              |
| Threshold dispersion after tuning | 10%                              |
| Maximum jitter                    | 25 ps at 10 fC                   |
| TDC contribution                  | < 10 ps                          |
| Time walk contribution            | < 10 ps                          |
| Dynamic range                     | 2.5 fC-100 fC                    |
| TDC conversion time               | < 25 ns                          |
| Trigger rate                      | 1 MHz L0 or 0.8 MHz L1           |
| Trigger latency                   | 10 μs L0 or 35 μs L1             |
| Clock phase adjustment            | 100 ps                           |

# Edge studies for Roman Pots: DRIE etching technique

- Non-sensitive area (edges) is critical for their applications in a Roman Pot
  - Current AC-LGADs have large non-active region → need optimization for application in Roman Pots
- Active edge provides a damage free interface that limits the extension of the dead silicon area, external to the sensitive
  area
  - o To be studied for AC-LGADs and compared to 3D detectors



**Deep reactive ion etching** technique provides low-damage trenches or columns in silicon.

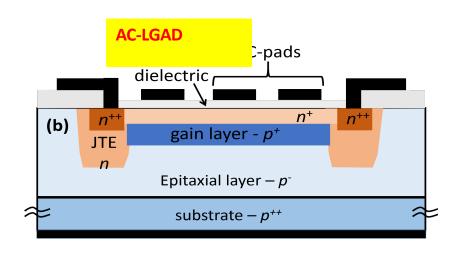
1:20 etch ratios are achievable. Any shape can be achieved.

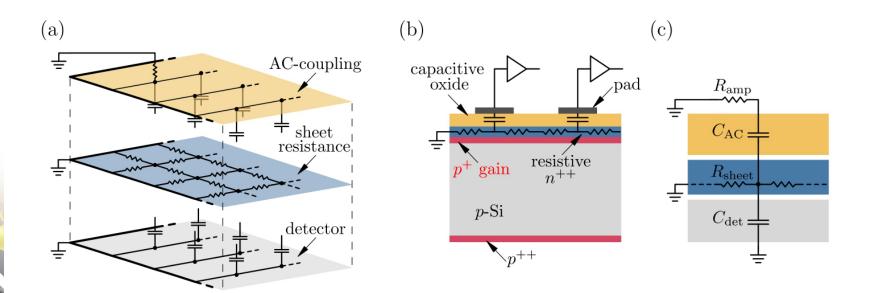
Surface needs passivation for damage removal, e.g. thermal oxidation.

To fabricate an active edge sensor, trenches must be etched all the way through the active thickness:

- For AC-LGADs, just 50 μm deep
- For 3D pixel sensors, ~ 200 μm

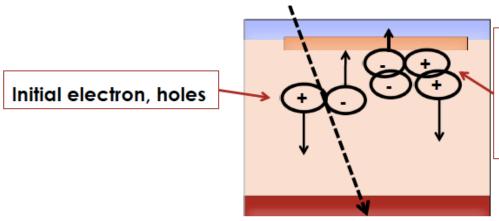
## AC-coupled LGAD





## Charge Multiplication in LGADs

N. Cartiglia

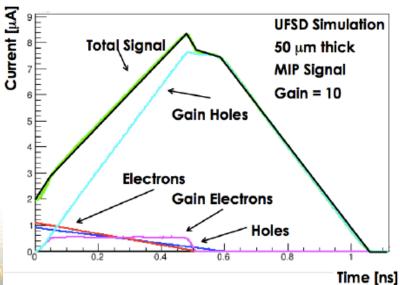


Gain electron:

absorbed immediately

Gain holes:

long drift home



Electrons multiply and produce additional electrons and holes.

- Gain electrons have almost no effect
- Gain holes dominate the signal
- → No holes multiplications

### Time Resolution in LGADs

N. Cartiglia

$$\sigma_{\rm t} = (\frac{\rm N}{{\rm dV/dt}})^2 + ({\rm Landau~Shap})^2$$

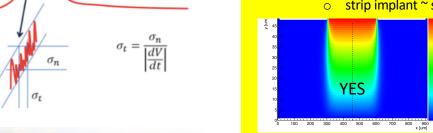
Usual "Jitter" term
Here enters everything that
is "Noise" and the
steepness of the signal

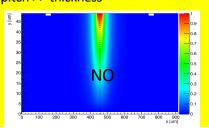
**Time walk**: Amplitude variation, corrected in electronics

**Shape variations:** non homogeneous energy

#### Signal Shape: **i∝qvE**<sub>w</sub>

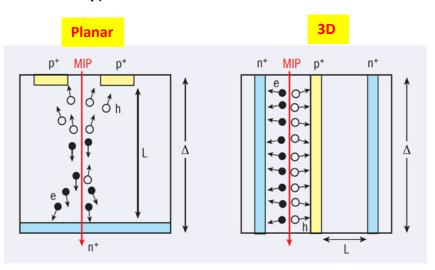
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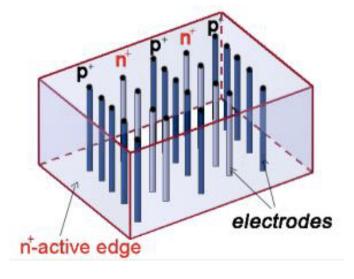
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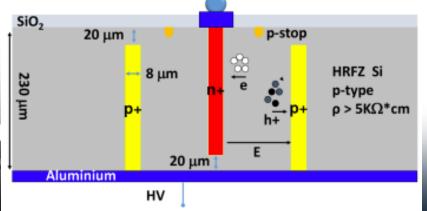
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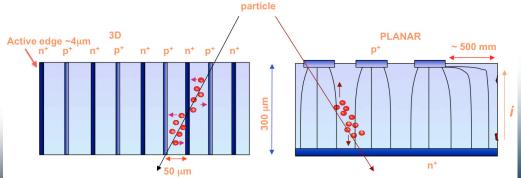
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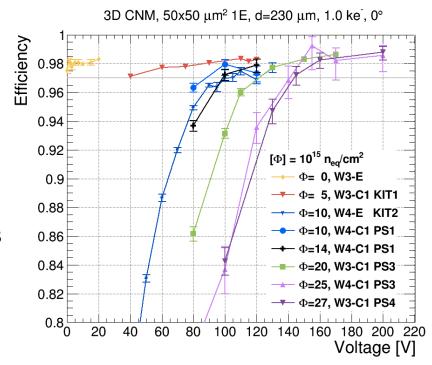




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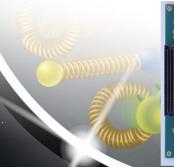






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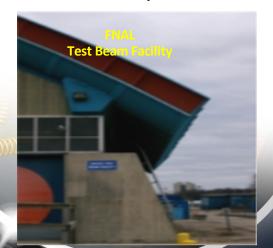






## FELIX and Caribou for Test Beams

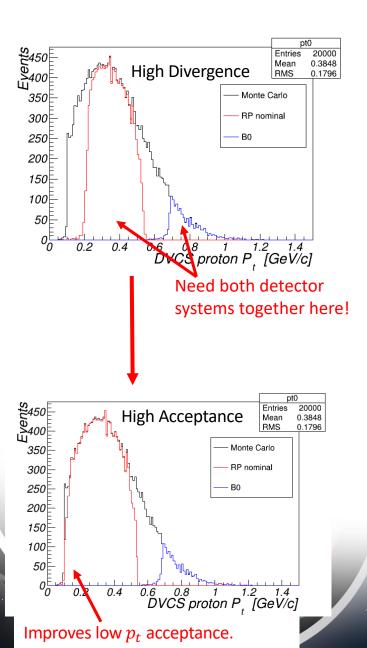
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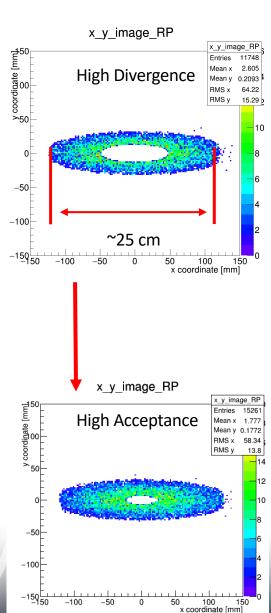


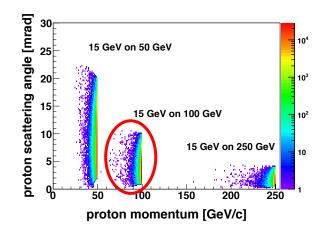
BNL's FELIX DAQ & CaRIBOu calibration boards used in this CERN test beam



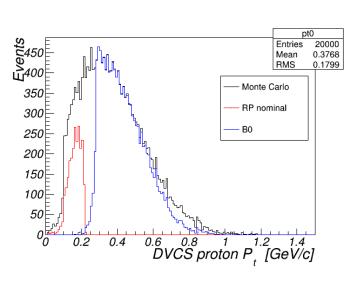
## 100 GeV DVCS protons

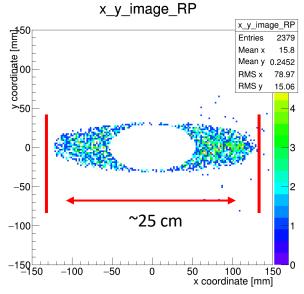


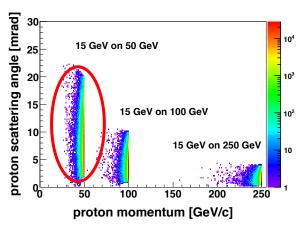




## 41 GeV DVCS protons



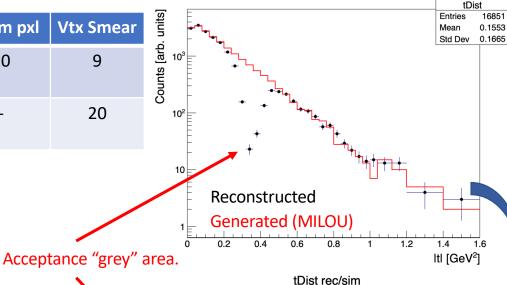




- Only one beam configuration for now.
- Acceptance gap still observed.
- Lower acceptance at high  $p_t$ .
- B0 plays largest role at this beam energy.

#### Momentum Resolution – 100 GeV

|                                 | Ang Div. | 20um pxl | 55um pxl | 500um pxl | Vtx Smear |
|---------------------------------|----------|----------|----------|-----------|-----------|
| Roman Pots $\Delta p_t$ [MeV/c] | 22       | -        | -        | 10        | 9         |
| B0 $\Delta p_t$ [Mev/c]         | 25       | 17       | 38       | -         | 20        |



t-distribution

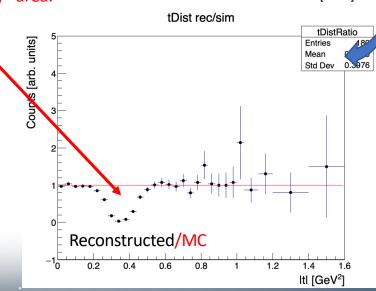
Total:

• RP:  $\Delta p_t \sim 23$  MeV/c (worst case)

• B0:  $\Delta p_t \sim$  26 MeV/c (20 um pixels)

• |t|-reconstruction requires combined Roman Pots and B0 information.

 Still allows reconstruction of |t|-dist since data points exist on both sides of gap.



## Momentum Resolution – 41 GeV

|                                 | Ang Div. | 20um pxl | 55um pxl | 500um pxl | Vtx Smear |
|---------------------------------|----------|----------|----------|-----------|-----------|
| Roman Pots $\Delta p_t$ [MeV/c] | 14       | N/A      | N/A      | 10        | 10        |
| B0 $\Delta p_t$ [Mev/c]         | 17       | 13       | 25       | N/A       | 10        |

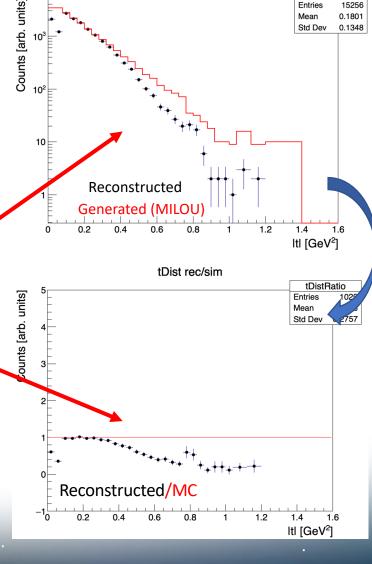


- RP:  $\Delta p_t \sim$  15 MeV/c (worse case)
- B0:  $\Delta p_t \sim$  18 MeV/c (20um pixels)
- |t|-reconstruction requires B0 for majority of reconstruction.

Some acceptance issues.

Optimization of BO sensor layout in **GEANT** ongoing.

Still need to optimize the location of the detectors.



t-distribution

tDist

0.1348